AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A microelectronic apparatus for performing $\underline{\otimes}$ multiplication and squaring in both polynomial based GF(2^q) and GF(p) field arithmetic, squaring and reduction using a serial fed radix 2^l multiplier, B, with k character multiplicand segments, A_i, and a k character $\underline{\oplus}$ accumulator wherein reduction to a limited congruence is performed "on the fly", in a systolic manner, with A_i, a multiplicand, times B, a multiplier, over a modulus, N, and a result being at most $2k + 1$ characters long, including the k first emitting disregarded zero characters, which are not saved, where k characters have no less bits than the modulus, the apparatus comprising;

a first (B), and second (N) main memory register means, each register operative to hold at least n bit long operands, respectively operative to store a multiplier value designated B, and a modulus, denoted N, wherein the modulus is smaller than 2n;

a digital logic sensing detector, Y0, operative to anticipate "on the fly" when a modulus value is to be $\oplus$ added to the value in the $\oplus$ adder accumulator device such that all first k characters emitting from the device are forced to zero;

a modular multiplying device for at least k character input multiplicands, with only one, at least k characters long $\underline{\oplus}$ adder, $\underline{\oplus}$ summation device operative to accept k character multiplicands, the $\underline{\otimes}$ multiplication device operative to switch into the $\underline{\oplus}$ accumulator device, in turn, multiplicand values, and in turn to receive multiplier values from a B register, and an "on the fly" simultaneously generated anticipated value as a multiplier which is operative to force k first emitting zero output characters in the first phase, wherein at each effective machine cycle at least one designated multiplicand is $\underline{\oplus}$ added into the $\underline{\oplus}$ accumulation device;

the multiplicand values to be switched in turn into the $\underline{\oplus}$ accumulation device consisting of one or two of the following three multiplicands, a ~~the~~ first multiplicand being an all-zero string value, a second multiplicand ~~value,~~ being the multiplicand A_i, and a third multiplicand being ~~value,~~ the N_0 segment of the modulus;

an apparatus to anticipate the l bit k character serial input Y_0 multiplier values;

the multiplier values which are input in turn into the multiplying device in the first phase being first the B operand, and concurrently, the second multiplier value consisting of the Y_0, "on the fly" anticipated k character string, to force first emitting zeroes in the output;

an $\underline{\oplus}$ accumulation device, operative to output values simultaneously as multiplicands are $\underline{\oplus}$ added into the $\underline{\oplus}$ accumulation device;

an output transfer mechanism, in the second phase operative to output a final modular $\underline{\otimes}$ multiplication result from the $\underline{\oplus}$ accumulation device,

wherein all addition, accumulation and multiplication operations are switchable to be performed either with carries or without carries, over GF(p) or over $GF(2^q)$.

2. (Original) An apparatus as in claim 1 wherein $\underline{\oplus}$ summations into the $\underline{\oplus}$ accumulation device are activated by each new serially loaded higher order multiplier characters.

3. (Original) An apparatus as in claim 1, wherein the multiplier characters;

are operative to cause no $\underline{\oplus}$ summation into the $\underline{\oplus}$ accumulation device if both the input B character and the corresponding input Y_0 character are zeroes;

are operative to $\underline{\oplus}$ add in only the A_i multiplicand if the input B character is a one and the corresponding Y_0 character is a zero;

are operative to $\underline{\oplus}$ add in only the N, modulus, if the B character is a zero, and the corresponding Y_0 character is a one; and

are operative to $\underline{\oplus}$ add in the $\underline{\oplus}$ summation of the modulus, N, with the multiplicand A_i if both the B input character and the corresponding Y_0 character are ones.

4. (Original) An apparatus as in claim 1, operative to preload multiplicand values A_i and N, into two designated preload buffers, and to $\underline{\oplus}$ summate these values into a

third multiplicand preload buffer, obviating the necessity of $\underline{\oplus}$ adding in each multiplicand value separately.

5. (Original) An apparatus as in claim 1, wherein the multiplier values are serial single character in input and the output of the $\underline{\oplus}$ accumulation device is serial single character output, wherein the Y_0 detect device is operative to anticipate only one character in a clocked turn.

6. (Original) An apparatus as in claim 1, wherein the $\underline{\oplus}$ accumulation device performs modulo 2, XOR addition/subtraction, wherein all carry bits in addition and subtraction components are disregarded, thereby precluding provisions for overflow and further limiting convergence in computations.

7. (Original) A $\underline{\otimes}$ multiplication apparatus as in claim 1 wherein all carry inputs are disabled to zero, denoted, S=0, typically operative to perform polynomial based multiplication.

8. (Original) An apparatus as in claim 1 wherein an S equal to zero acting on an element in a circuit equation computing in GF(2^q), the S designates omitted circuitry and all adders and subtractors, designated $\underline{\oplus}$ have been reduced to XOR, modulo 2 addition/subtraction elements.

9. (Original) An apparatus as in claim 1 wherein k first emitting zeroes will egress from the device controlled by the following four quantities in anticipating the next in turn Y_0 character:

i. the l bit S_{out} bits of the result of the l bit by l bit mod 2^l $\underline{\otimes}$ multiplication of the right-hand character of the A_i register times the B_d character of the B Stream, $A_0 \cdot B_d \bmod 2^l$;

ii. the first emitting carry out character from the $\underline{\oplus}$ accumulation device, S(CO_0);

iii. the l bit S_{out} character from the second from the right character emitting cell of the $\underline{\oplus}$ accumulation device, SO_1;

iv. the l bit J_0 value, which is the negative multiplicative inverse of the right-hand character in the N_0 modulus multiplicand register.

wherein values, $A_0 \cdot B_d \bmod 2^l$, $S(CO_0)$, and SO_1 are $\underline{\oplus}$ added character to character together and "on the fly" multiplied by the J_0 character to output a valid Y_0 zero-forcing anticipatory character to force an l bit egressing string of zeroes.

10. (Original) An apparatus as in claim 1, wherein $\underline{\otimes}$ multiplication on polynomial based operands is performed in a reverse mode, multiplying from right hand MS characters to left hand LS characters, operative to perform modular reduced $\underline{\otimes}$ multiplication without Montgomery type parasitic functions.

11. (Original) An apparatus as in claim 1 where the preload buffers are serially fed and where multiplicand values are preloaded into the preload buffers on the fly from a multiplicity of memory devices.

12. (Original) An apparatus as in claim 1, wherein a previous value, emitting from an additional n bit register, S, is $\underline{\oplus}$ summated into the output value of the $\underline{\oplus}$ accumulation device via an l bit $\underline{\oplus}$ adder circuit such that first emitting output characters are zeroes when the Y_0 detector is operative to detect the necessity of $\underline{\oplus}$ adding moduli to the $\underline{\oplus}$ summation in the $\underline{\oplus}$ accumulation device, wherein the Y_0 detector is operative to detect utilizing the next in turn $\underline{\oplus}$ added characters $A_0 \cdot B_d \bmod 2^l$, $S(CO_0)$, SO_1, S_d and $S(CO_2)$, the composite of $\underline{\oplus}$ added characters to be finite field $\underline{\otimes}$ multiplied on the fly by the l bit J_0 value, where $\underline{\oplus}$ defines the addition and $\underline{\otimes}$ defines the multiplication as befits the finite field used in the process.

13. (Original) An apparatus as in claim 1, wherein for $l = 1$, J_0 is implicitly 1, and the J_0 $\underline{\otimes}$ multiplication is implicit, without additional hardware.

14. (Original) An apparatus as in claim 1 wherein a comparator is operative to sense a finite field output from the $\underline{\otimes}$ modular multiplication device, working in GF(p), where the first right hand emitting k zero characters are disregarded, where the output is larger than the modulus, N, thereby operative to control a modular reduction whence said value is output from the memory register to which the output stream from the multiplier device is destined, and thereby precluding allotting a second memory storage device for the smaller product values.

15. (Original) A device as in claim 1 wherein for $\underline{\otimes}$ modular multiplication in the GF(2^q), the apparatus is operative to multiply without an externally precomputed more than l bit zero-forcing factor.

16. (Original) A method according to claim 1 operative to compute a J_0 constant by resetting either the A operand value or the B operand value to zero and setting the partial result value, S_0, to 1.

17. (Currently Amended) A microelectronic apparatus for performing interleaved finite field $\underline{\otimes}$ modular multiplication of integers A and B operative to generate an output stream of A times B modulus N wherein n the number of characters in the modulus operand register is larger than k, wherein the $\underline{\otimes}$ multiplication process is performed in iterations, wherein at each interleaved iteration with operands input into a $\underline{\otimes}$ multiplying device, consisting of N, the modulus, B, a multiplier, a previously computed partial result, S, and a k character string segment of A, a multiplicand, the segments progressing from the A_0 string segment to the A_{m-1} string segment, wherein each iterative result is $\underline{\oplus}$ summated into a next in turn S, temporary result, in turn, wherein first emitting characters of iterative results are zeroes, the apparatus comprising:

first (B), second (S) and third (N) main memory registers, each register capable of storing and outputting operands, respectively operative to store a multiplier value, a partial result value and a modulus, also denoted N;

a modular multiplying device operative to $\oplus$ summate into the $\oplus$ accumulation device, in turn one or two of a plurality of multiplicand values, in turn, during the phases of the iterative $\otimes$ multiplication process, and in turn to receive as multipliers, in turn, inputs from a first value B register, second, from an "on the fly" anticipating value, Y_0, as a multiplier to force first emitting right-hand zero output characters in each iteration, and third values from the modulus, N, register;

the multiplicand parallel registers operative at least to receive in turn, values from the A, B, and N register sources, and in turn, also a multiplicand zero forcing Y_0, value;

a first emitting zero forcing Y_0 detect device operative to generate a binary string operative to be a multiplier during the first phase and operative to be a multiplicand in the second phase;

multiplicand values to be switched into the accumulation device for the first phase consisting of a first zero value, a second value, A_i, which is a k character string segment of a multiplicand, A, and a third value N_0, being the first emitting k characters of the modulus, N;

a temporary result value, S, resulting from a previous iteration, operative to be summated with the value emanating from the accumulation device, to generate a partial result for the next in turn iteration;

multiplicand values to be input, in turn, into the accumulation device for the second phase being, a first zero value, a second A_i operand, remaining in place from the first phase, and a third Y_0 value having been anticipated in the first phase;

multiplier values input into the multiplying device in the first phase being a first emitting string, B_0, being the first emitting string segment of the B operand, concurrently multiplying with the second multiplier value consisting of the anticipated Y_0 string which is simultaneously loaded character by character as it is generated into a preload multiplicand buffer for the second phase;

the two multiplier values input into the apparatus during the second phase being the left hand $n - k$ character values from the B operand, designated B, and the left hand $n - k$ characters of the N modulus, designated N, respectively; and

a multiplying flush out device operative in the last phase to transfer the left hand segment of a result value remaining in the accumulation device into a result register,

wherein multiplication on polynomial based operands is performed in a reverse mode, multiplying from MS characters to LS characters, operative to perform modular reduction without Montgomery type parasitic functions.

18. (Cancelled)

19. (Currently Amended) An apparatus according to claim 17 operative to anticipate the Y_0 value using first emitting values of the multiplicand, and present inputs of the B multiplier, carry out values from the accumulation device, summation values from the accumulation device, the present values from the previously computed partial result, and carry out values from an ~~the~~ adder which summates the result from the accumulation device with the previous partial result.

20. (Currently Amended) An apparatus as in claim 19 wherein k first emitting zeroes will egress from the device controlled by the following six quantities in anticipating the next in turn Y_0 character:

i. the l bit S_{out} bits of the result of the l bit by l bit mod 2^l multiplication of the right-hand character of ~~the~~ A_i ~~register~~ times the B_d character of the B operand ~~Stream~~, $A_0 \cdot B_d$ mod 2^l;

ii. the first emitting carry out character from the accumulation device, $S(CO_0)$;

iii. the l bit S_{out} character from the second from the right-hand character emitting cell of the accumulation device, SO_1;

iv. the next in turn character value from the S stream, S_d;

v. the l bit carry out character from the Z output full adder, $S(CO_z)$;

vi. the l bit J_0 value, which is the negative multiplicative inverse of the right-hand character in the N_0 modulus multiplicand register;

wherein values, $A_0 \cdot B_d \bmod 2^l$, $S(CO_0)$, SO_1, S_d are added character to character together and "on the fly" multiplied by the J_0 character to output a valid Y_0 zero-forcing anticipatory character to force an l bit egressing character string of zeroes.

21. (Original) An apparatus as in claim 17 comprised of at least one sensor operative to compare the output result to N, the modulus, the mechanism operative to actuate a second subtractor on the output of the result register, thereby to output a modular reduced value which is limited congruent to the output result value precluding the necessity to allot a second memory storage for a smaller result.

22. (Original) An apparatus as in claim 17 where a value which is a summation of two multiplicands is loaded into a preload character buffer with at least a k characters memory means register concurrently whilst one of the values is loaded into a preload buffer.

23. (Original) An apparatus with only one accumulation device, and an anticipating zero forcing mechanism operative to perform a series of interleaved modular multiplications and squarings concurrently performing the equivalent of three natural integer multiplication operations, such that a result is an exponentiation.

24. (Original) An apparatus as in claim 17 where next in turn used multiplicands are preloaded into preload register buffer means on the fly.

25. (Original) An apparatus as in claim 17 where a value which is a summation of two multiplicands is summated into at least a k character register concurrently whilst one of the values is loaded into its preload buffer.

26. (Original) An apparatus as in claim 17 wherein apparatus buffers and registers are operative to be loaded with values from external memory sources and said buffers and registers are operative to be unloaded into the external memory source during

computations, such that the maximum size of the operands is dependent on available memory means.

27. (Original) An apparatus as in claim 17 wherein memory register means are typically serial single character in/serial single character out, parallel at least *k* characters in/parallel at least *k* characters out, serial single character in/parallel at least *k* characters out, and parallel *k* characters in/serial single character out.

28. (Original) An apparatus as in claim 17 wherein the final phase of a multiplication type iteration, the multiplier inputs are zero characters operative to flush out the left hand segment of the carry save accumulator memory.

29. (Original) An apparatus as in claim 17 where next in turn used multiplicands are preloaded into preload memory buffers on the fly.

30. (Original) An apparatus as in claim 17 where multiplicand values are preloaded into the preload buffers on the fly from central storage memory means.

31. (Currently Amended) A microelectronic apparatus for performing modular multiplication, squaring and reduction, the apparatus multiplying a multiplicand A by a multiplier B over a modulus N, wherein B is a serial fed radix 2^l multiplier comprising no more than k character multiplier segments, A comprises no more than k character multiplicand segments, and N has no more than k characters, each character having l bits, the apparatus comprising:

a first (B) register operative to store the multiplier B;

a modular multiplication device accepting multiplicands having no more than k characters, the modular multiplication device including a single accumulation device at least k characters long and operative to repeatedly receive a multiplicand and simultaneously output a character;

a digital logic sensing detector operative to anticipate that a non-zero character would be about to be output from the single accumulation device and to determine a number of times, Y_0, that the modulus N should be added into the single accumulation device so as to force the non-zero character to zero,

the modular multiplication device operative, during a first phase, to switch into the single accumulation device, in turn, multiplicand values, and to receive, character by character, the contents of the B register and the Y_0 value from the digital logic sensing detector, thereby to force up to k first output characters which are zero, the multiplicand values switched in turn into the accumulation device comprising less than 3 of the following three multiplicands: (a) an all-zero string value; (b) a portion of the multiplicand A; and (c) at least a portion of the modulus N; and

an output transfer mechanism, operative in a last phase to unload at least a portion of a final modular multiplication result from the accumulation device,

wherein all addition, accumulation and multiplication operations are switchable to be performed either with carries or without carries, over GF(p) or over $GF(2^q)$.

32. (Original) Apparatus according to claim 31 for performing interleaved modular multiplication and reduction in a plurality of interleaved iterations, wherein the Y_0 value used in the first phase is saved, and wherein said portion of the modulus N comprises a k-character least significant portion thereof,

the apparatus also comprising a second (S) register operative to store a temporary result S from an iteration I for use during a subsequent iteration i+1 and a third (N) register operative to store the modulus N, wherein n, the number of characters in the third (N) register, is larger than k;

the modular multiplication device being operative, in a first phase, to multiply a plurality of slices of A during the plurality of interleaved iterations respectively, by B,

the modular multiplication device being operative, during a second phase between the first and last phases, to switch into the single accumulation device, in turn, multiplicand values, and to receive multiplier values from the B and N registers, the multiplicand values switched in turn into the accumulation device comprising less than 3 of the following three multiplicands: (a) an all-zero string value; (b) a portion of the multiplicand A; and (c) the Y_0 value as saved from the first phase;

the apparatus also comprising a serial addition device operative, during each iteration, to summate the temporary result value S in the second (S) register with the character output by the accumulation device, thereby to generate n-k least significant characters of a new temporary result, which characters are stored in the second (S) register, for the next in turn iteration.

33. (Cancelled)

34. (Original) Apparatus according to claim 31 which employs Y_0 as the next character of a polynomial based modular reducing quotient deterministically.

35. (Original) An apparatus as in claim 31 wherein the digital logic sensing detector is operative to receive the following four inputs:

i. the product of the least significant character in the A register multiplied by a current value from the B register, in modulus 2^l;

ii. the first emitted carry out character from the accumulation device;

iii. the contents of the second from the right character in the accumulation device;

iv. the negative multiplicative inverse of the right-hand character in the N register.

36. (Original) An apparatus as in claim 32 wherein the digital logic sensing detector is operative to receive the following six inputs:

i. the product of the least significant character in the A register multiplied by a current value from the B register, in modulus 2^l;

ii. the first emitted carry out character from the accumulation device;

iii. the contents of the second from the right character in the accumulation device;

iv. the negative multiplicative inverse of the right-hand character in the N register.

v. the next in turn character in the S register; and

vi. the carry out character from the serial addition device.

37. (Currently Amended) A method for performing modular multiplication, squaring and reduction, including multiplying a multiplicand A by a multiplier B over a modulus N, wherein B is a serial fed radix 2^l multiplier comprising no more than k character multiplier segments, A comprises no more than k character multiplicand segments, and N has no more than k characters, each character having l bits, the method comprising:

storing a multiplier B in a first (B) register;

providing a modular multiplication device accepting multiplicands having no more than k characters, the modular multiplication device including a single

accumulation device at least k characters long and operative to repeatedly receive a multiplicand and simultaneously output a character;

anticipating that a non-zero character would be about to be output from the single accumulation device and determining a number of times, Y_0, that the modulus N should be added into the single accumulation device so as to force the non-zero character to zero,

during a first phase, switching into the single accumulation device, in turn, multiplicand values, and receiving, character by character, the contents of the B register and the Y_0 value from the digital logic sensing detector, thereby to force up to k first output characters which are zero, the multiplicand values switched in turn into the accumulation device comprising less than 3 of the following three multiplicands: (a) an all-zero string value; (b) a portion of the multiplicand A; and (c) at least a portion of the modulus N; and

in a last phase, unloading a final modular multiplication result from the accumulation device,

wherein all addition, accumulation and multiplication operations are switchable to be performed either with carries or without carries, over GF(p) or over $GF(2^q)$.

38. (Original) A method according to claim 37 for performing interleaved modular multiplication and reduction in a plurality of interleaved iterations, wherein the Y_0 value used in the first phase is saved, and wherein said portion of the modulus N comprises a k-character least significant portion thereof, the method also comprising:

providing a second (S) register operative to store a temporary result S from an iteration i for use during a subsequent iteration i+1 and a third (N) register operative to store the modulus N, wherein n, the number of characters in the third (N) register, is larger than k;

the modular multiplication device being operative, in the first phase, to multiply a plurality of slices of A during the plurality of interleaved iterations respectively, by B,

the modular multiplication device being operative, during a second phase between the first and last phases, to switch into the single accumulation device, in turn, multiplicand values, and to receive multiplier values from the B and N registers, the multiplicand values switched in turn into the accumulation device comprising less than 3 of the following three multiplicands: (a) an all-zero string value; (b) a portion of the multiplicand A; and (c) the Y_0 value as saved from the first phase,

the method also comprising summating, during each iteration, the temporary result value S in the second (S) register with the character output by the accumulation device, thereby to generate a new temporary result, for the next in turn iteration.

39. (Cancelled)

40. (Original) A method according to claim 37 which deterministically employs Y_0 as the next character of a polynomial based modular reducing quotient.